PRP

INTERFACE MANUAL

ROCKWELL
84900-00
50019

LCDAC 12

PRESTON

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CONTENTS

DESCRIPTION — SECTION

PART I - SYSTEM DESCRIPTION

BROCHURES AND SPECIFICATIONS 1

PRODUCT DATA SHEETS

SYSTEM SPECIFICATIONS

BLOCK DIAGRAM 2

SYSTEM INTERCONNECT INFORMATION 3

SYSTEM INTERCONNECT DRAWING

WIRE LIST

SHIPPING KIT

PART II - SYSTEM OPERATION AND PROGRAMMING

FRONT PANEL OPERATION 4

INTERFACE 5

INTERFACE OPERATION AND PROGRAMMING (HP 12006A)

PART III - TEST REPORTS

CONTENTS

DESCRIPTION SECTION

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SYSTEM INTERCONNECTION INFORMATION 3

SYSTEM INTERCONNECTING DRAWING

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INTERFACE 5

INTERFACE OPERATION AND PROGRAMMING (HP 12005A)

PART III - TEST REPORTS

TAB PRODUCTS CO.
1450 East 17th St., Suite 218
Santa Ana, CA 92701
(714) 558-0464

MODEL LCDAC12 SPECIFICATIONS

Resolution:	12 Binary Bits
Input Code:	Two's Complement
Linearity Error:	±½ LSB Max.
Differential Linearity:	±3/4 LSB Max.
Gain Error:	Adjustable to ±.01% FS
Zero Error:	Adjustable to ±.01% FS
Monotonicity:	Monotonic over temperature range 0° to 50°C
Settling time to final value	
±.01% FS:	
For FSR Step	15 microseconds
For 1 LSB Step	5 microseconds
±.05% FSR Step	5 microseconds
Slew Rate:	10V/usec
Control:	2 Rank Registers
	Rank 1 - Input storage register Rank 2 - DAC input register
Typical glitch amplitude:	< 70 mV
Analog Output:	±10V FS
Output Current:	5 mA Max.
Drift: (Includes gain, zero, linearity)	±.004% FS/°C
Logic:	Positive True TTL
Package:	2 channels/card

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MODEL LCDAC12 SPECIFICATIONS

Operating Temperature:	0 to 50°C
Storage Temperature:	-20° to 80°C
System Packaging:	Up to 64 channels in one Model GM-3 Card Module complete with power supply.
System Operation: (Reference: Figure 1)	Single or Dual Rank Operation

Data is entered into individually addressed input registers (Rank 1) with a data strobe. It is then immediately loaded into the corresponding DAC input register (Rank 2) for single rank operation. For dual rank operation, all Rank 2 input registers are simultaneously loaded with a common XFR strobe.

Address distributor logic is included so one common set of data lines plus channel address lines can be used to control all D/A channels.

A DAC controller chassis with front panel switches is required for systems with over 64 channels and is optional on other systems. This allows the user to manually load data into any channel without using the computer.

NOTE: The D/A Converters are intended to be used in a Preston card module with appropriate mating connectors and power supplies.

MODEL LCDAC12 SPECIFICATIONS

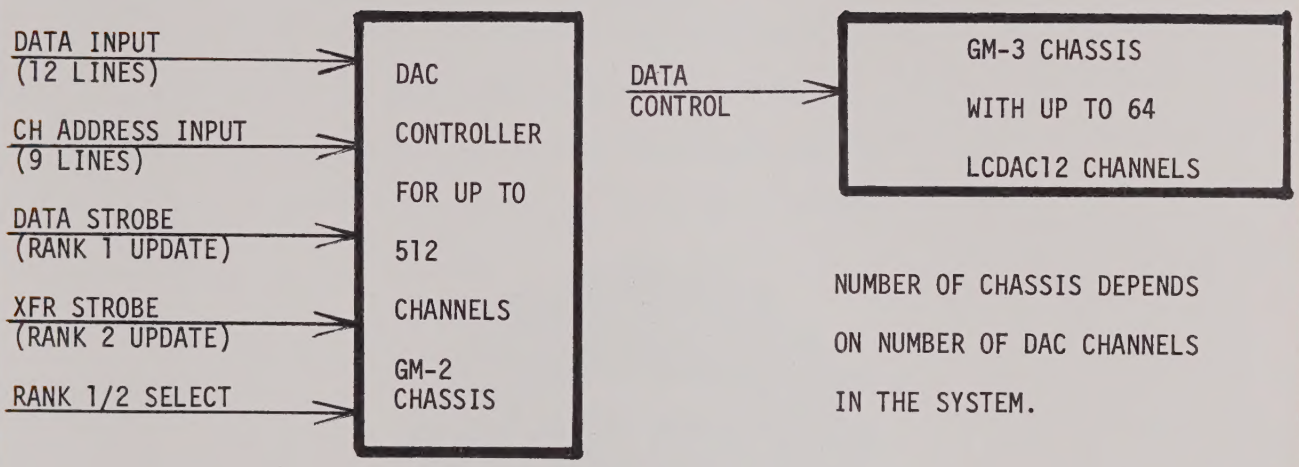

FIGURE 1

CHASSIS DIMENSIONS:	Width (GM-2 or GM-3)	19	Inches
	Height (GM-2 or GM-3)	5.25	Inches
	Depth (GM-2)*	20	Inches
	(GM-3)*	26.5	Inches

*Includes Mating Connectors

Preston Scientific
Leaders in the development and manufacture of
precision amplifiers and analog-to-digital
conversion systems since 1959.

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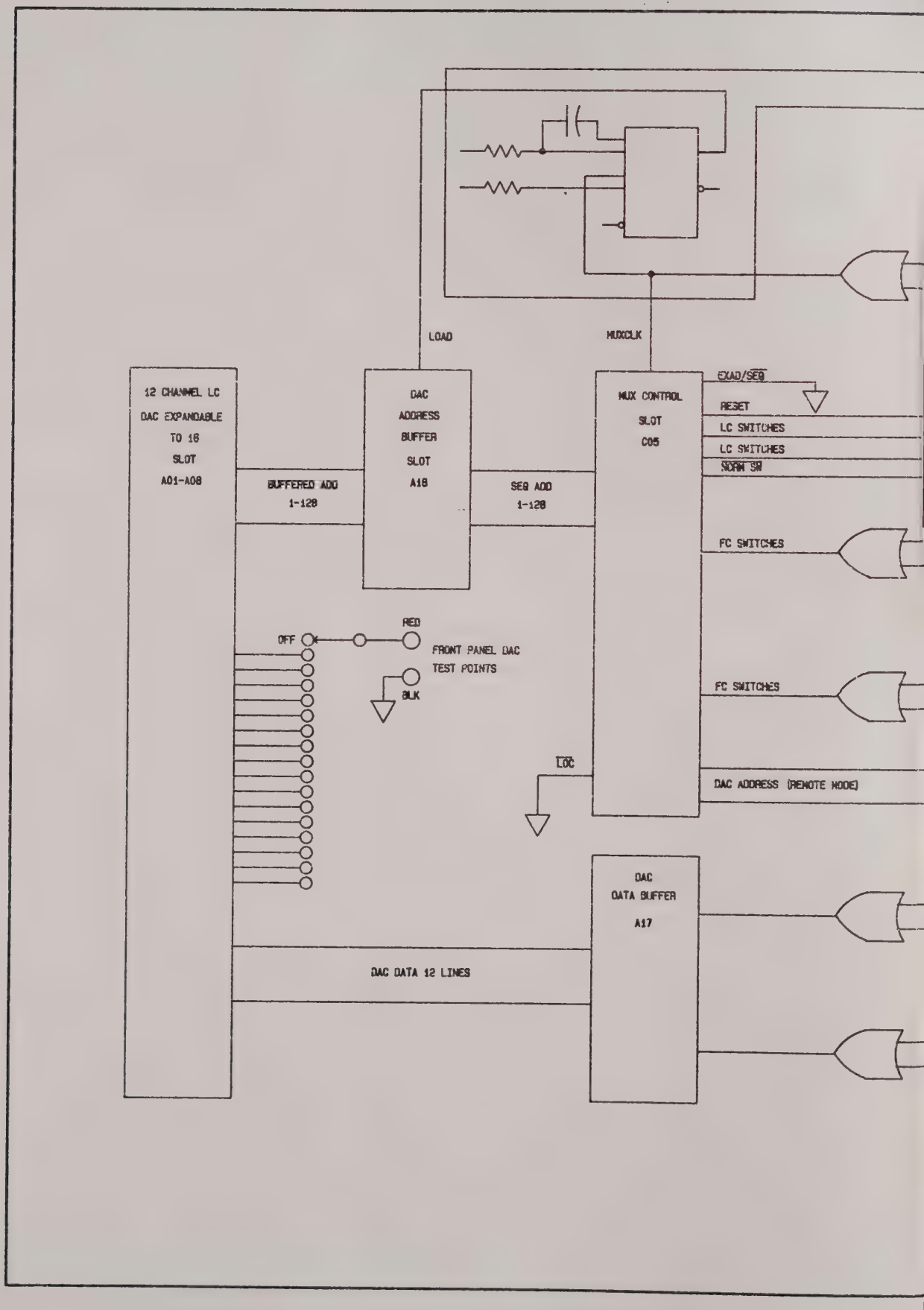
Preston Scientific
805 E. Cerritos Avenue, Anaheim, California 92805
Telephone (714) 776-6400 Telex: 5101004596

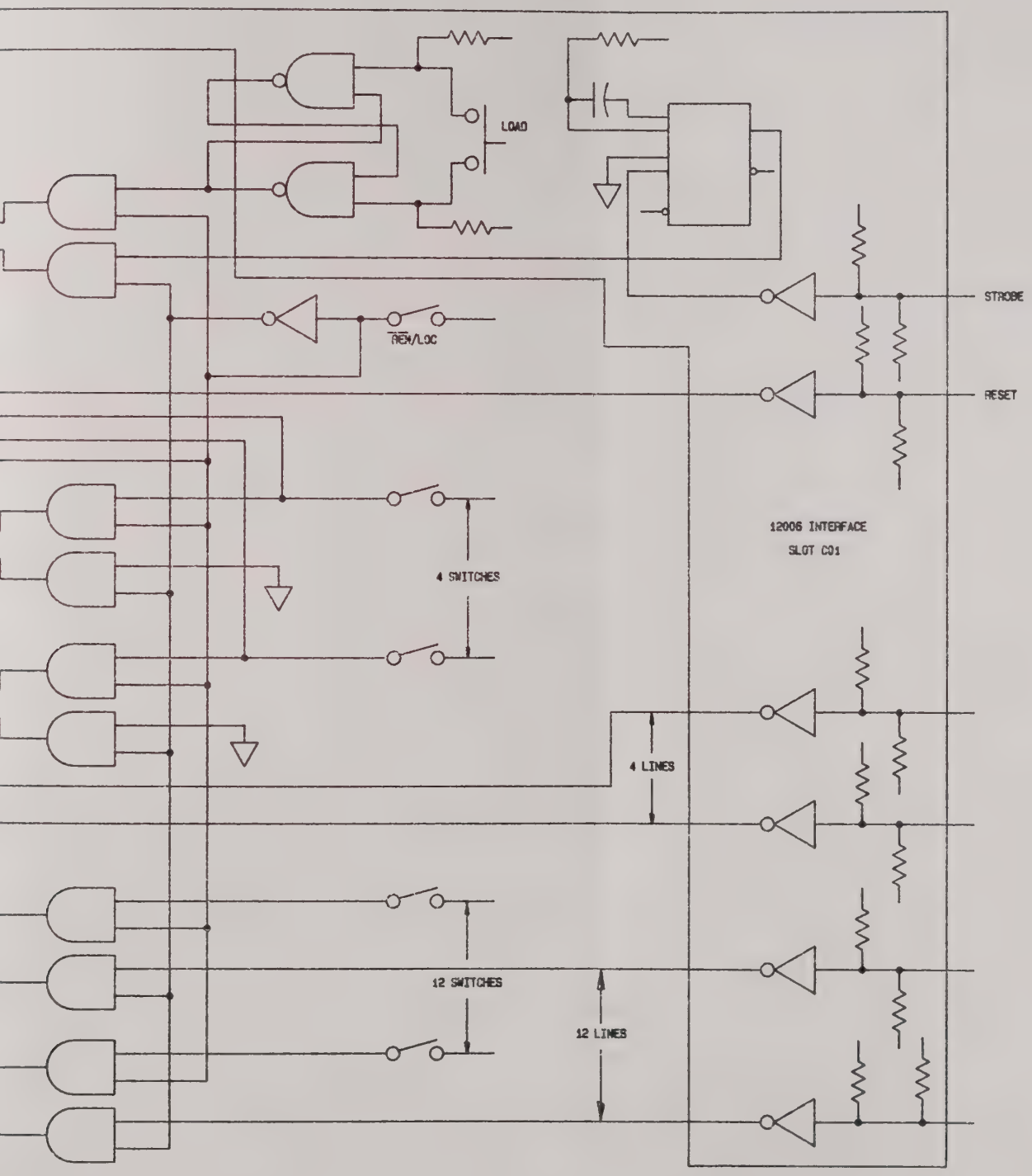
Printed in U.S.A.

GM Series Digital-to-Analog Conversion System model DACRS12/16 consisting of..

12 each:	Model LCDAC12-12B D/A Converter
1 each:	Model GMDAC Controller
1 each:	Interface with hardware compatibility to HP12006A
OUTPUT:	12 Channels of D/A Converter.
EXPANSION:	Pre-wired for 16 channels total.
FULL-SCALE:	+/- 10 Volts at 5 mA per channel.
RESOLUTION:	11 binary bits and sign.
INPUT CODE:	Two's complement.
INTERFACE/ CONTROL:	Hardware compatible with HP12006A.
LOGIC:	TTL, Compatible with interface.
SPECIAL FEATURES:	A. Sequential operation in remote mode.
	B. Remote/Local switch.
	C. Random Channel Addressing (Binary) for inputting data (two's complement format) via front panel.
POWER:	117 VRMS +/- 10%, 60 Hz.

LIBRARY OF CONGRESS

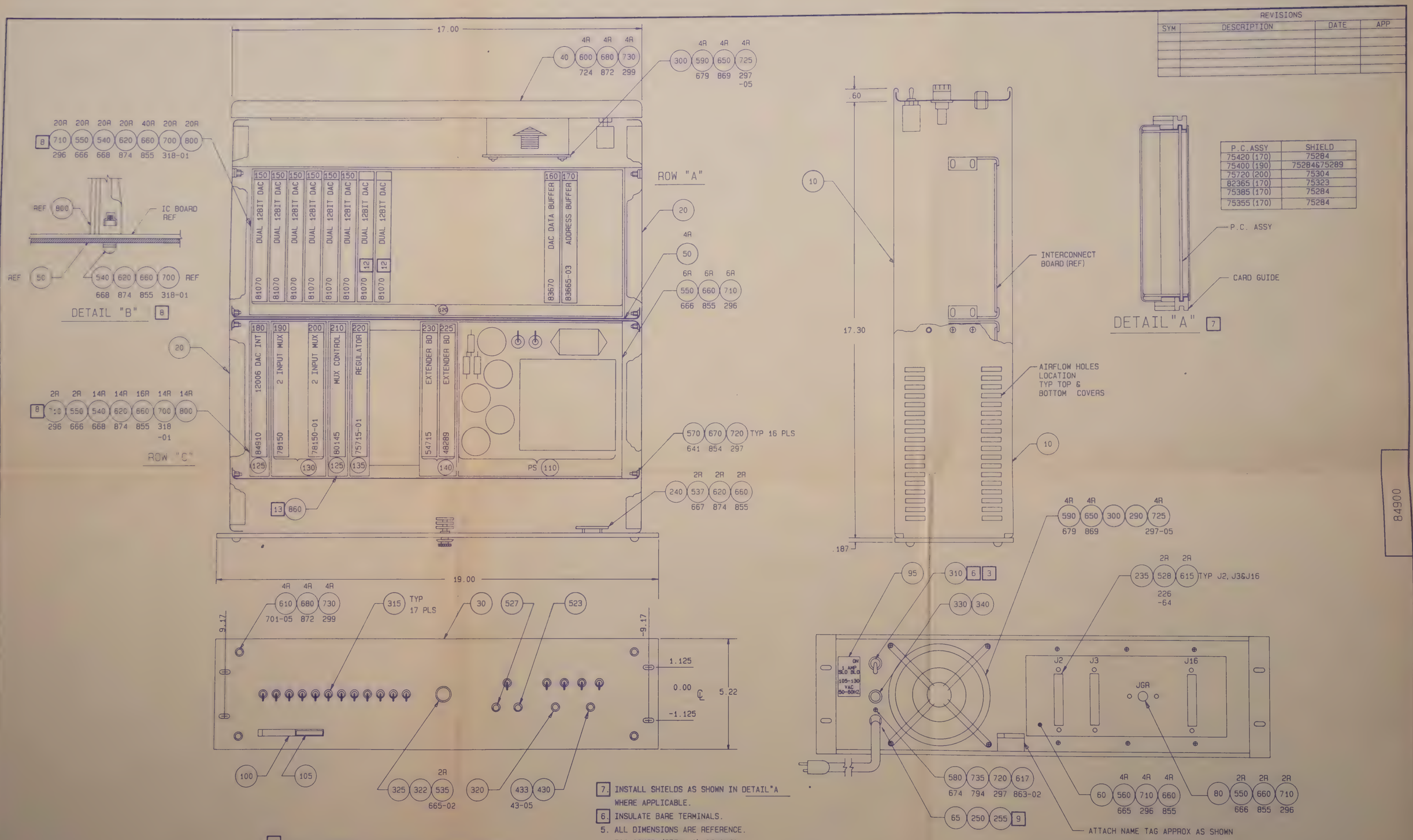

LOAD
MUXCLK
12 CHANNEL LC
DAC EXPANDABLE
TO 16
SLOT
A01-A08
DAC
ADDRESS
BUFFER
SLOT
A18
MUX CONTROL
SLOT
C05
EXAD/SEQ
RESET
LC SWITCHES
LC SWITCHES
NORM SW
BUFFERED ADD
1-128
SEQ ADD
1-128
FC SWITCHES
RED
OFF
FRONT PANEL DAC
TEST POINTS
BLK
FC SWITCHES
LOC
DAC ADDRESS (REMOTE MODE)
DAC
DATA BUFFER
A17
DAC DATA 12 LINES



BLOCK DIAGRAM P/N 84900 PRESTON

TAB PRODUCTS CO.
1450 East 17th St., Suite 218
Santa Ana, CA 92701

REVISIONS			
SYM	DESCRIPTION	DATE	APP



P.C.ASSY	SHIELD
75420 (170)	75284
75400 (190)	75284&75289
75720 (200)	75304
82365 (170)	75323
75385 (170)	75284
75355 (170)	75284

13. INSTALL CONNECTOR (ITEM 860) ON COMPONENT SIDE.
12. WIRED FOR EXPANSION. DO NOT INSTALL.
11. FOR FRONT PANEL REFERENCE DESIGNATIONS SEE DWG NO. 84920.
10. FOR SHIPPING KIT SEE DWG NO. 81359.
9. INSTALL SPACER (ITEM 65) ON INSIDE OF REAR PANEL.
8. INSTALL CARD GUIDES (ITEM 800) AS SHOWN IN DETAIL "B" WHERE APPLICABLE.

7. INSTALL SHIELDS AS SHOWN IN DETAIL"A" WHERE APPLICABLE.
6. INSULATE BARE TERMINALS.
5. ALL DIMENSIONS ARE REFERENCE.
4. TOP COVER (ITEM 10) REMOVED FOR CLARITY ON TOP VIEW.
3. MOUNT KEYWAY DOWN (ITEM 310).
2. FOR USER CONNECTION, SIGNAL LIST, CONNECTOR LIST AND GLOSSARY SEE DWG NO. N/A.
1. FOR WIRE LIST SEE DWG NO. 84902.

NOTE: UNLESS OTHERWISE SPECIFIED.

BY		DATE
DWN	SON TRAN	1-28
CHK		
ENG		
APP		
NEXT ASSY		

T10

TITLE: 12CH LC DAC 12BIT EXP TO 16, +/-10V.F.S. 5MA, TWO'COMPLEMENT

4773.1986

PRESTON

84900

SH 1 OF 3

84900

FROM	TO

WIRE LIST PIN CONNECTION LOCATION INFORMATION

THE WIRE LIST PIN DESIGNATIONS ARE REFERENCED TO INPUT/OUTPUT CONNECTORS AS WELL AS THE INTERCONNECT CARDS, FRONT PANEL SWITCHES, POTENTIOMETERS, AND TEST POINTS. THE FOLLOWING INFORMATION DESCRIBES THE NOMENCLATURE DESIGNATIONS AND THEIR MEANING.

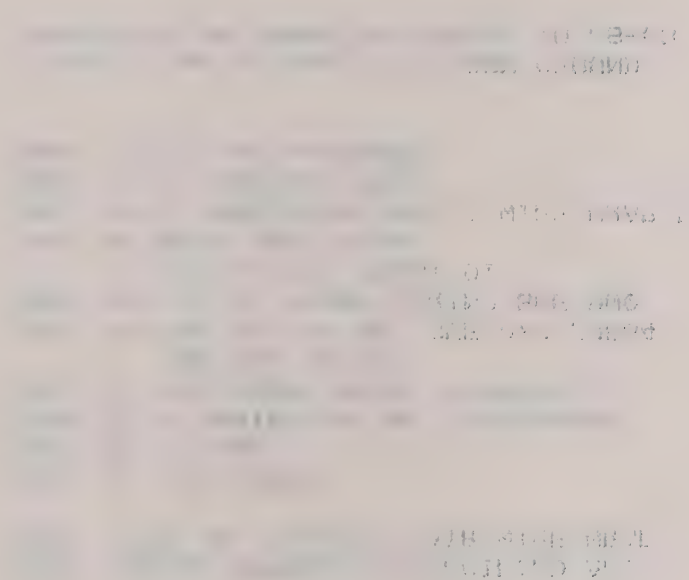
	SECTION DESIGNATION				
	PIN			PIN	
SIGNAL NAME	XX	XX	SIGNAL NAME	XX	XX

SECTIONS ARE DESCRIBED AS FOLLOWS

J = INDICATES CONNECTOR
S = INDICATES SWITCH
R = INDICATES POTENTIOMETER
TP = INDICATES TEST POINT

A, B, C, D, ETC. INDICATES INTERCONNECT BOARD

		FROM	TO
10	P	WIRE LIST, 12 CHANNELS LC DAC 12 BIT	
20	1	P/N 84902-00	
30	2	NOTE UNLESS OTHERWISE SPECIFIED ALL	
40		WIRE IS TO BE TWISTED PAIR WIRE WRAP	
50	1	NOTE 01 WIRE WRAP	
60		NOTE 02 22 AWG	
70		NOTE 03 * INDICATES THE COMPLEMENT	
80		NOTE 04 FOR FRONT PANEL REFERENCE	
90		DWG SEE 84920	
100		NOTE 05 FOR SWITCH S19 SEE DWG 80864	
110		NOTE 06 FOR AC POWER WIRING SEE DWG	
120		54826-01 & 56061-01	
130		NOTE 07 WIRE WRAP COAX	
140		NOTE 08 % INDICATES DOUBLE WIRE WRAP PIN	
150		NOTE 09 24 AWG BUS WIRE	
160		NOTE 10 18 AWG SOLDERED	
170	2	CONNECT TWO 22 AWG WIRE FROM GROUND	
180		POST ON REAR CONNECTOR PLATE TO PS-03	



		FROM	TO		
190	P	CONNECTOR J2 DIGITAL INPUTS			
200	1	ADD 8	J2 A19 ADD 8*	C01 37W	
210		GRD	J2 B19 GRD	C02 29	
220		ADD 4	J2 B22 ADD 4*	C01 36W	
230		GRD	J2 A22 GRD	C02 29	
240		ADD 2	J2 B20 ADD 2*	C01 35W	
250		GRD	J2 A20 GRD	C02 29	
260		ADD 1	J2 A23 ADD 1*	C01 34W	
270		GRD	J2 B23 GRD	C02 29	
280		DA256 BIT6	J2 A13 DA 256*	C01 47W	
290		GRD	J2 B13 GRD	C02 29	
300		DA512 BIT5	J2 A03 DA 512*	C01 48W	
310		GRD	J2 B02 GRD	C02 29	
320		DA1024 BIT4	J2 B14 DA 1024*	C01 49W	
330		GRD	J2 A14 GRD	C02 29	
340		DASIGN BIT3	J2 B04 DA SIGN*	C01 50W	
350		GRD	J2 A04 GRD	C02 29	
360		RESET	J2 B24 RESET*	C01 33W	
370		GRD	J2 A24 GRD	C02 29	
380		STROBE	J2 B10 STROBE*	C01 32W	NOTE 07
390		GRD	J2 A10 GRD	C02 29	NOTE 07

		FROM			TO		
400	P	CONNECTOR J3 DIGITAL INPUTS					
410	1	DA01	BIT14	J3 A21	DA01*	C01	39W
420		GRD		J3 B21	GRD	C02	29
430		DA02	BIT13	J3 B19	DA02*	C01	40W
440		GRD		J3 A19	GRD	C02	29
450		DA04	BIT12	J3 B11	DA04*	C01	41W
460		GRD		J3 A11	GRD	C02	29
470		DA08	BIT11	J3 A10	DA08*	C01	42W
480		GRD		J3 B10	GRD	C02	29
490		DA16	BIT10	J3 B08	DA16*	C01	43W
500		GRD		J3 A08	GRD	C02	29
510		DA32	BIT 9	J3 A18	DA32*	C01	44W
520		GRD		J3 B18	GRD	C02	29
530		DA64	BIT 8	J3 B22	DA64*	C01	45W
540		GRD		J3 A22	GRD	C02	29
550		DA128	BIT 7	J3 B25	DA128*	C01	46W
560		GRD		J3 A25	GRD	C02	29

		FROM	TO
570	P	CONNECTOR J16 ANALOG OUTPUTS	
580	1	DACOT 01	J16 A12 CHAN 0 A01 30
590		DACOT 01 SH	J16 A11 CHAN 0 SH A01 31
600		DACOT 02	J16 A10 CHAN 1 A01 32
610		DACOT 02 SH	J16 A11 CHAN 1 SH A01 33
620		DACOT 03	J16 A09 CHAN 0 A02 30
630		DACOT 03 SH	J16 A08 CHAN 0 SH A02 31
640		DACOT 04	J16 A07 CHAN 1 A02 32
650		DACOT 04 SH	J16 A08 CHAN 1 SH A02 33
660		DACOT 05	J16 A06 CHAN 0 A03 30
670		DACOT 05 SH	J16 A05 CHAN 0 SH A03 31
680		DACOT 06	J16 A04 CHAN 1 A03 32
690		DACOT 06 SH	J16 A05 CHAN 1 SH A03 33
700		DACOT 07	J16 A03 CHAN 0 A04 30
710		DACOT 07 SH	J16 A02 CHAN 0 SH A04 31
720		DACOT 08	J16 A01 CHAN 1 A04 32
730		DACOT 08 SH	J16 A02 CHAN 1 SH A04 33
740		DACOT 09	J16 B12 CHAN 0 A05 30
750		DACOT 09 SH	J16 B11 CHAN 0 SH A05 31
760		DACOT 10	J16 B10 CHAN 1 A05 32
770		DACOT 10 SH	J16 B11 CHAN 1 SH A05 33
780		DACOT 11	J16 B09 CHAN 0 A06 30
790		DACOT 11 SH	J16 B08 CHAN 0 SH A06 31
800		DACOT 12	J16 B07 CHAN 1 A06 32
810		DACOT 12 SH	J16 B08 CHAN 1 SH A06 33
820		DACOT 13	J16 B06 CHAN 0 A07 30
830		DACOT 13 SH	J16 B05 CHAN 0 SH A07 31
840		DACOT 14	J16 B04 CHAN 1 A07 32
850		DACOT 14 SH	J16 B05 CHAN 1 SH A07 33
860		DACOT 15	J16 B03 CHAN 0 A08 30
870		DACOT 15 SH	J16 B02 CHAN 0 SH A08 31
880		DACOT 16	J16 B01 CHAN 1 A08 32
890		DACOT 16 SH	J16 B02 CHAN 1 SH A08 33
900		PWRGRD	J16 B13 PWR GRD A06 37
910		PWRGRD	J16 A13 PWR GRD A06 37

		FROM	TO	
920	P	FRONT PANEL WIRING		
930		SEE NOTE 4 & 5		
940	1	MANUAL DATA ENTRY		
950	1	SIGN	S17 C1 INSW 5	C02 15 NOTE 01
960		1024	S16 C1 INSW 6	C02 18 NOTE 01
970		512	S15 C1 INSW 7	C02 21 NOTE 01
980		256	S14 C1 INSW 8	C02 24 NOTE 01
990		128	S13 C1 INSW 9	C02 30 NOTE 01
1000		64	S12 C1 INSW 10	C02 37 NOTE 01
1010		32	S11 C1 INSW 11	C02 34 NOTE 01
1020		16	S10 C1 INSW 1	C04 02 NOTE 01
1030		8	S09 C1 INSW 2	C04 05 NOTE 01
1040		4	S08 C1 INSW 3	C04 11 NOTE 01
1050		2	S07 C1 INSW 4	C04 08 NOTE 01
1060		1	S06 C1 INSW 5	C04 15 NOTE 01
1070	2	DAC ADDRESS		
1080	1	8	S04 C1 INSW 1	% C02 02 NOTE 01
1090		4	S03 C1 INSW 2	% C02 05 NOTE 01
1100		2	S02 C1 INSW 3	% C02 11 NOTE 01
1110		1	S01 C1 INSW 4	% C02 08 NOTE 01
1120	2	LOAD SWITCH		
1130	1	LOAD NC	S18 NC LNC	C01 23W NOTE 01
1140		LOAD NO	S18 NO LNO	C01 24W NOTE 01
1150		LOAD C	S18 C GRD	C02 29 NOTE 01
1160	2	LOCAL/REMOTE SWITCH		
1170	1	LOC/REM*	S05 C1 LOC/REM*	% C02 13 NOTE 01
1180		LOC/REM*	S05 B1 GRD	C02 29 NOTE 01
1190	1	DIGGRD	S01 A1 DIGGRD	S02 A1 NOTE 09
1200		DIGGRD	S02 A1 DIGGRD	S03 A1 NOTE 09
1210		DIGGRD	S03 A1 DIGGRD	S04 A1 NOTE 09
1220		DIGGRD	S04 A1 DIGGRD	C02 29 NOTE 02
1230	1	DIGGRD	S06 A1 DIGGRD	S07 A1 NOTE 09
1240		DIGGRD	S07 A1 DIGGRD	S08 A1 NOTE 09
1250		DIGGRD	S08 A1 DIGGRD	S09 A1 NOTE 09
1260		DIGGRD	S10 A1 DIGGRD	S11 A1 NOTE 09
1270		DIGGRD	S11 A1 DIGGRD	S12 A1 NOTE 09
1280		DIGGRD	S12 A1 DIGGRD	S13 A1 NOTE 09

	FROM		TO		
1290	DIGGRD	S13 A1	DIGGRD	S14 A1	NOTE 09
1300	DIGGRD	S14 A1	DIGGRD	S15 A1	NOTE 09
1310	DIGGRD	S15 A1	DIGGRD	S16 A1	NOTE 09
1320	DIGGRD	S16 A1	DIGGRD	S17 A1	NOTE 09
1330	DIGGRD	S17 A1	DIGGRD	C02 29	NOTE 02

		FROM			TO		
1340	P	OUTPUT MONITOR					
1350	1	DAOT 1	S19	A2	DAOT 1	A01 30	NOTE 01
1360		DAOT 2	S19	A3	DAOT 2	A01 32	NOTE 01
1370		DAOT 3	S19	A4	DAOT 3	A02 30	NOTE 01
1380		DAOT 4	S19	A5	DAOT 4	A02 32	NOTE 01
1390		DAOT 5	S19	A6	DAOT 5	A03 30	NOTE 01
1400		DAOT 6	S19	A7	DAOT 6	A03 32	NOTE 01
1410		DAOT 7	S19	A8	DAOT 7	A04 30	NOTE 01
1420		DAOT 8	S19	A9	DAOT 8	A04 32	NOTE 01
1430		DAOT 9	S19	A10	DAOT 9	A05 30	NOTE 01
1440		DAOT 10	S19	A11	DAOT 10	A05 32	NOTE 01
1450		DAOT 11	S19	A12	DAOT 11	A06 30	NOTE 01
1460		DAOT 12	S19	A13	DAOT 12	A06 32	NOTE 01
1470		DAOT 13	S19	A14	DAOT 13	A07 30	NOTE 01
1480		DAOT 14	S19	A15	DAOT 14	A07 32	NOTE 01
1490		DAOT 15	S19	A16	DAOT 15	A08 30	NOTE 01
1500		DAOT 16	S19	A17	DAOT 16	A08 32	NOTE 01
1510		WIPER	S19	WPR	DAOUT	TP1	NOTE 01
1520		GRD	A04	37	DAGRD	TP2	NOTE 02
1530	2	POWER ON					
1540	1	+15V	LDI	1	LED	C01 30W	
1550		GRD	LDI	2	LEDGRD	C01 25W	

		FROM			TO		
1560	P			INTERCONNECT WIRING			
1570				SEE NOTE 01 UNLESS OTHERWISE NOTED			
1580	1	SIGN		C01 20W	INCC 5	C02 14	
1590		1024		C01 19W	INCC 6	C02 17	
1600		512		C01 18W	INCC 7	C02 22	
1610		256		C01 17W	INCC 8	C02 23	
1620		128		C01 16W	INCC 9	C02 26	
1630		64		C01 15W	INCC 10	C02 38	
1640		32		C01 14W	INCC 11	C02 35	
1650		16		C01 13W	INCC 1	C04 01	
1660		8		C01 12W	INCC 2	C04 04	
1670		4		C01 11W	INCC 3	C04 12	
1680		2		C01 10W	INCC 4	C04 09	
1690		1		C01 09W	INCC 5	C04 14	
1700		AD 8		C01 07W	MUXAD 8	C05 34W	
1710		AD 4		C01 06W	MUXAD 4	C05 33W	
1720		AD 2		C01 05W	MUXAD 2	C05 32W	
1730		AD 1		C01 04W	MUXAD 1	C05 31W	
1740		RESET		C01 03W	RESET	C05 35C	
1750		STROBE		C01 02W	INCC 6	C04 17	NOTE 07
1760		STROBE SH		C01 02C	STROBE SH	C04 29	NOTE 07
1770		L		C01 22W	INSW 6	C04 18	
1780		OT 6	%	C04 19	MUXCLK	C05 23C	
1790		OT 6	%	C04 19	MUXCLK	C01 31W	NOTE 07
1800		OT 6 SH		C04 29	MUXCLK SH	C01 ~~31W~~ 26W	NOTE 07
1810		LOAD		C01 1W	LOAD	A18 26	NOTE 07
1820		LOAD SH		C02 ~~29~~ 4	LOAD SH	A18 29	NOTE 07
1830		SIGN		C02 16	SIGN	A17 35	
1840		1024		C02 19	1024	A17 36	
1850		512		C02 20	512	A17 37	
1860		256		C02 25	256	A17 34	
1870		128		C02 27	128	A17 31	
1880		64		C02 36	64	A17 30	
1890		32		C02 33	32	A17 32	
1900		16		C04 3	16	A17 33	
1910		8		C04 6	8	A17 25	
1920		4		C04 10	4	A17 24	
1930		2		C04 7	2	A17 27	
1940		1		C04 16	1	A17 26	
1950		GRD		C02 29	GRD	A17 29	
1960		GRD		C02 29	GRD	A17 29	
1970		OT 1 8		C02 03	FCSW	C05 39W	
1980		OT 2 4		C02 06	FCSW	C05 38W	
1990		OT 3 2		C02 10	FCSW	C05 37W	
2000		OT 4 1		C02 07	FCSW	C05 36W	
2010		INCC 1		C02 01	GRD	C02 29	
2020		INCC 2		C02 04	GRD	C02 29	
2030		INCC 3		C02 12	GRD	C02 29	
2040		INCC 4		C02 09	GRD	C02 29	

	FROM		TO		
2050	INSW 1 8	C02 02	LCSW 8	C05 44W	
2060	INSW 2 4	C02 05	LCSW 4	C05 43W	
2070	INSW 3 2	C02 11	LCSW 2	C05 42W	
2080	INSW 4 1	C02 08	LCSW 1	C05 41W	
2090	SEQADD 1	C05 18W	ADD 1	A18 35	
2100	SEQADD 2	C05 19W	ADD 2	A18 37	
2110	SEQADD 4	C05 20W	ADD 4	A18 32	
2120	SEQADD 8	C05 21W	ADD 8	A18 31	
2130	SEQADD 16	C05 22W	ADD 16	A18 16	
2140	SEQADD 32	C05 21C	ADD 32	A18 34	
2150	SEQADD 64	C05 22C	ADD 64	A18 20	
2160	SEQADD 128	C05 16W	ADD 128	A18 17	
2170	FCSW 32	C05 30C	MUXAD 16	C05 35W	
2180	MUXAD 16	C05 35W	MUXAD 32	C05 39C	
2190	MUXAD 32	C05 39C	MUXAD 64	C05 40C	
2200	MUXAD 64	C05 40C	FCSW 16	C05 40W	
2210	FCSW 16	C05 40W	FCSW 64	C05 42C	
2220	FCSW 64	C05 42C	LCSW 32	C05 43C	
2230	LCSW 32	C05 43C	LCSW 64	C05 44C	
2240	LCSW 64	C05 44C	LCSW 128	C05 45C	
2250	LCSW 128	C05 45C	LCSW 16	C05 45W	
2260	LCSW 16	C05 45W	LCSW 128	C05 47C	
2270	FCSW 128	C05 47C	MCP BNC	C05 47W	
2280	MCP BNC	C05 47W	MUXAD 128	C05 48C	
2290	MUXAD 128	C05 48C	NORM SW*	C05 49C	
2300	LOC*	C05 49C	GRD	C02 29	
2310	MUXEN	C05 23W	GRD	C02 29	
2320	INCC 7	C04 22	INSW 7	C04 21	
2330	INSW 7	C04 21	GRD	C04 29	
2340	LOC/REM* %	C02 13	LOC/REM*	C04 13	
2350	EN*	C02 32	EN*	C04 32	
2360	LOC/REM*	C04 13	NORM SW*	C05 48W	
2370	BAD 1	A18 36	ADD 1	A16 09	
2380	SHIELD	PS 09	PWRGRD	PS 03	NOTE 02
2390	EN*	C04 32	GRD	C04 29	
2400	EXTADD	C05 30W	GRD	C02 29	
2410	NORM MODE	C05 24W	CRAN SW*	C05 50W	

		FROM		TO		
2420	P	POWER SUPPLY & GROUND WIRING				
2430		SEE NOTE 02				
2440	1	INTERCONNECT ROW 'A'				
2450	1	+10V	A01 28	+10V	PS 10	
2460		+22V	A16 38	+22V	PS 11	
2470		-22V	A16 36	-22V	PS 12	
2480		DIGGRD	A01 29	PWRGRD	PS 03	
2490		PWRGRD	A16 37	PWRGRD	PS 02	
2500		PWRGRD	A01 37	PWRGRD	PS 03	
2510	2	INTERCONNECT ROW 'C'				
2520	1	+10V	C01 28	+10V	PS 10	
2530		+10V	C02 28	+10V	PS 10	
2540		+10V	C04 28	+10V	PS 10	
2550		+10V	C06 28	+10V	PS 10	
2560		+5V	C06 22	+5V	C05 28	
2570		GRD	C06 18	PWRGRD	C05 26	
2580		GRD	C06 18	PWRGRD	PS 03	
2590		GRD	C02 29	PWRGRD	PS 03	
2600		GRD	C02 29	PWRGRD	PS 03	
2610		GRD	C01 26	PWRGRD	PS 03	
2620		GRD	C01 26	GRD	C02 29	NOTE 10
2630		GRD	C02 29	GRD	C05 26	NOTE 10
2640		GRD	C05 26	GRD	C06 18	NOTE 10

TITLE: SHIPPING KIT
DWG NO. 81359-00 REV .....
SHEET....OF....

PRESTON SCIENTIFIC
PRINTED 06/05/87

PARTS LIST

ITEM	QTY	PART NO.	DESCRIPTION
40	1	681-01	SCREW PHMS 8-32 X 1/4
50	1	871-00	WASHER FLAT #8

TAB PRODUCTS CO.
1400 East [illegible]
[illegible]
714 [illegible]

DATA SWITCHES

Data Switches are used in the local mode, to set up the data word for DAC Data, Control Word, Clock Divisor, First Channel, and Last Channel.

RUN / STOP / STEP SWITCH

RUN — After the system has been programmed, move the switch up to the RUN position, and the system will start and continue running.

STOP — When the system is running and you wish to halt the process, move the switch to the STOP position, and the system will stop. (If running in the sequential mode, the system will stop after completion of last channel.)

STEP — In sequential mode, depress the switch to the STEP position to enter DAC data and step the channel address to the next address.

NOTE: The RUN / STOP / STEP switch is only functional in the local mode.

Media Switches are used in the local mode. To set up the media type for
VAC Data: Control Word: Clock Divisor : First Channel, or Count Clear

Wait_2_TICK_2 (Other Functions)

switch up to the VGA position, and the system will
start the counting sequence.

STOP When the system is running and you wish to k le
the process, move the switch to the STOP position,
and the system will stop. (If running in the
assembly mode, the system will stop after
completion of the task chosen.)

START In setting to mode, depress the switch to the "ON"
position. Enter the data via the chosen
address to the next address.

The MOV / Jump / Short switch is only functional in the

CONTROL WORD

Depress (CONTROL WORD) to select the operating mode. Depress (REMOTE / LOCAL / ENTER) to ENTER. This enters the mode into storage.

DATA

Depress (DATA) to select DAC data. Depress (REMOTE / LOCAL / ENTER) to ENTER. This enters DAC data on the channel addressed.

ADDRESS

Depress (ADDRESS) to select the desired channel. Depress (REMOTE / LOCAL / ENTER) to ENTER. This enters the desired channel address.

CLOCK DIVISOR

Depress ((CLOCK DIVISOR) to select the desired divisor. Depress (REMOTE / LOCAL / ENTER) to ENTER. This enters the desired divisor.

LAST CHANNEL

Depress (LAST CHANNEL) to select the desired last channel in a sequential mode. Depress (REMOTE / LOCAL / ENTER) to ENTER. This enters the desired last channel.

FIRST CHANNEL

Depress (FIRST CHANNEL) to select the desired first channel in a sequential mode. Depress (REMOTE / LOCAL / ENTER to ENTER. This enters the desired first channel.

Press (CONTROL-ALT-D) to select the operating mode
Depress (CANCEL / LOCAL / ENTER) to ENTER. This
enters the mode into storage.

Depress (ENTER) to select DAC code. Depress (CANCEL
the decimal code used.

Depress (CANCEL / LOCAL / ENTER) to ENTER.

Depress (CANCEL / LOCAL / ENTER) to ENTER
enters the desired division.

Depress (CTRL-ALT-D) to select the desired last
record in [illegible] mode. Depress (RECORD /
LOCAL / ENTER) to ENTER. This enters the desired
last record.

LOCAL / ENTER) to ENTER. This enters the desired

REMOTE / LOCAL / ENTER SWITCH

Switch in Remote, system is controlled by external device.

Switch in Local, system is controlled by Front Panel Switches.

Enter, Depress switch to ENTER position to enter data for selected control modes.

I/O CONTROL WORD DEFINITION

MODE OR FUNCTION	MSB----------CONTROL WORD----------LSB															
		32K	16K	8K	4K	2K	1K	512	256	128	64	32	16	8	4	2	1
SPECIAL-(32K)																	
LOCAL LOCKOUT-(16K)																	
REMOTE/LOCAL* (REG)-(8K)																	
CLRDAC-(4K)																	
EXT/INT* (CLOCK SOURCE)-(2K)																	
BURST/CHANNEL RATE*(CLK MODE)-(1K)																	
CAMEN/CAMBY*-(512)																	
SEQ/RANDOM*-(256)																	
XFR(8) (PROG TRANSFER)-(128)																	
XFR(7) (EXT TRANSFER)-(64)																	
CLOCK DIVISOR-(32)																	
FIRST ADDRESS-(16)																	
LAST ADDRESS-(8)																	
CAM WRITE-(4)																	
CONTROL HANDSHAKE ENABLE-(2)																	
CONTROL WORD EXTENSION--(1)																	

RANDOM MODE

Depress (CONTROL WORD)

Set data switches to all zero's.

Depress (ENTER)

Set (RUN / STOP / STEP) switch to RUN.

Set (RUN / STOP / STEP) to STOP.

Depress (ADDRESS)

Set data switches for desired address.

Depress (ENTER)

Depress (DATA)

Set data switches for desired data.

Depress (ENTER) to enter data.

SEQUENTIAL MODE

Depress (CONTROL WORD)

Set data switches for sequential mode.

Depress (ENTER FIRST CHANNEL)

Set data switches for desired first channel.

Depress (ENTER)

Depress (LAST CHANNEL)

Set data switches for desired last channel.

Depress (ENTER)

Depress (CLOCK DIVISOR)

Set data switches greater than 32.

Depress (ENTER)

Depress (DATA)

Set data switches to all zero's.

Set (RUN / STOP / STEP) to RUN.

Depress (ADDRESS)

Running channels are being displayed.

Set (RUN / STOP / STEP) to STOP.

Last channel is displayed.

Set data switches to desired data.

Depress (STEP)

Mux advances to First Channel and enters data into first rank registers. Set data switches to desired data.

Depress (STEP)

The DAC will load the first rank register for this channel.

Repeat until Last Channel is reached.

When the Last Channel is reached, the DAC will then copy the first rank registers into the second rank registers for all channels, updating the analog outputs.

To enter the same data into all channels, set data switches to the desired data.

Set (RUN / STOP / STEP) to RUN.

Set (RUN / STOP / STEP) to STOP.

TAB PRODUCTS CO.
1450 East 17th St., Suite 218
Santa Ana, CA 92701
(714) 558-0464

GM SERIES

DIGITAL-TO-ANALOG

CONVERSION SYSTEM

PART NUMBER_____

MODEL NUMBER_____

SERIAL NUMBER_____

SECTION 1 DIGITAL-TO-ANALOG CONVERTER
FUNCTIONAL DESCRIPTION ____ 1
SPECIFICATIONS ____ 1

SECTION 2 SYSTEM DESCRIPTION
DUAL RANK REGISTER ____ 2

SECTION 3 CALIBRATION

Our Address Is: PRESTON SCIENTIFIC
805 East Cerritos Avenue
Anaheim, California 92805

Our Telephone No. Is: (714) 776-6400

Our EasyLink address is:

from other EasyLink users. . .

Preston's EasyLink mailbox address 62879399

from other Telex or TWX user's. . .
Preston's Telex and Answer Back numbers

Telex 5101004596
Answer Back 5101004596ESL UD

DIGITAL-TO-ANALOG CONVERTER

FUNCTIONAL DESCRIPTION

The Model GM Series Digital-to-Analog Converter is a solid state instrument that will upon command produce an analog representation of a digital input binary word.

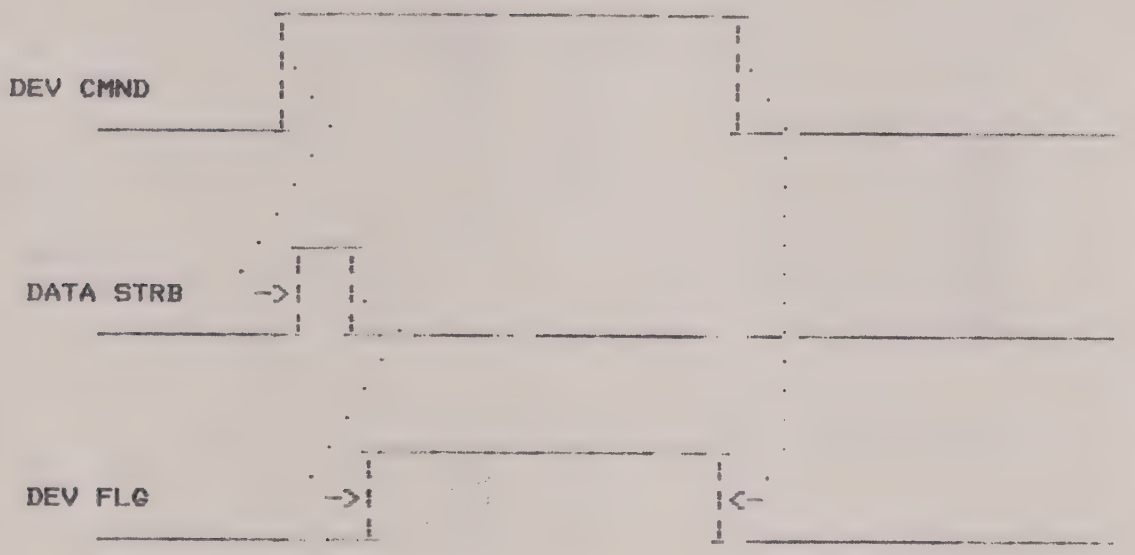
GENERAL SPECIFICATIONS

RESOLUTION: 12 binary bits.
CONVERSION RATE: 1 mHz maximum (digital update).
INPUT MEMORY: 1K FIFO
DATA CODE: two's complement.
OUTPUT VOLTAGE: ±10.
OUTPUT CURRENT: Up to +5 milliamps short circuit protected.
ANALOG SETTLING TIME: Less than 15 microseconds from a 20 volt step to within 0.01% of full scale and less than 5 microseconds for a 1 LSB step to within 0.01% of full scale.
LOGIC LEVELS: Positive true TTL.
CONTROL: Dual Rank Registers.
Rank 1 - Input storage register
Rank 2 - DAC input register
GLITCH AMPLITUDE: < 70 mV (typical)
POWER REQUIREMENT: 110 volts AC 50-60 Hz.
OPERATING TEMPERATURE: 0C to 50C.
SIZE: 20 to 26.5 inches in depth, 19 inches wide, and 5.25 inches in height.

SYSTEM CONTROL

DUAL RANK REGISTER

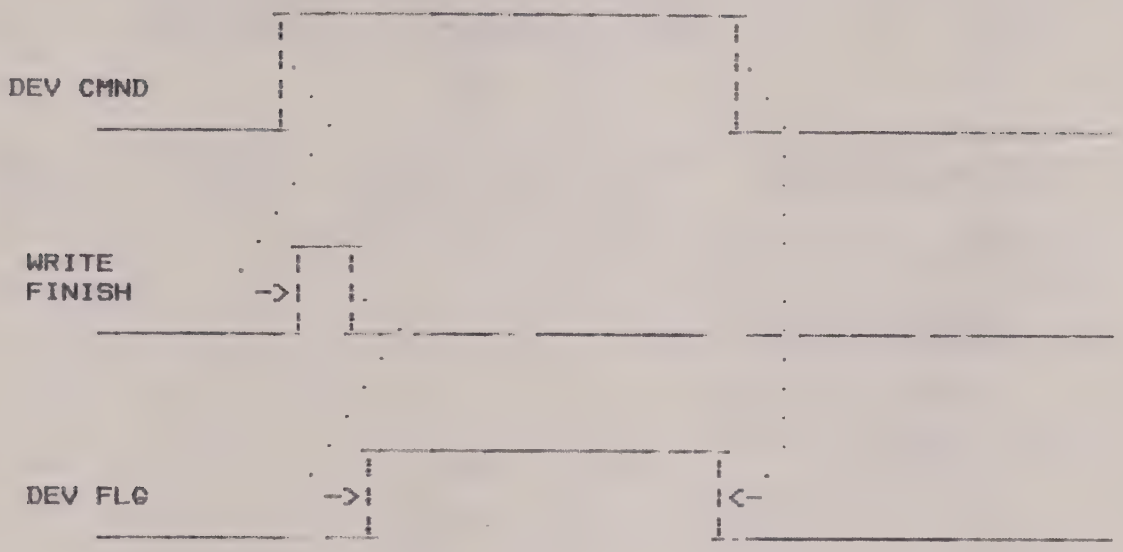
IN the dual rank input configuration, there are two "D" flip-flop registers, one after the other. The LOAD pulse loads the digital input data from the customer's data lines into the first register. The TRANSFER pulse transfers the contents of the first register into the second register. The output of the second register directly drives the DAC. In this manner, the customer's different digital data can be stored in the first register of each DAC channel (mulitple DAC system) and tha application of the TRANSFER pulse applied to all second registers, all the DAC outputs can update simultaneously. Other variations of the use of these registers may be customer specified.



Rising edge of DEV CMND creates DATA STRB.

Falling edge of DATA STRB causes DEV FLG to go HI.

Falling edge of DEV CMND causes DEV FLG to go LO.



Rising edge of DEV CMND creates WRITE FINISH.

Falling edge of WRITE FINISH causes DEV FLG to go HI.

Falling edge of DEV CMND causes DEV FLG to go LO.

SYSTEM DESCRIPTION

****
* 4 BIT CONTROL WORD TRUTH TABLE *
****

(CTRL 3) BIT 15	(CTRL 2) BIT 14	(CTRL 1) BIT 13	(CTRL 0) BIT 12	MODE DESCRIPTION
0	0	0	0	RUN WHILE LOADING FIFO
0	0	0	1	SET FIRST CHANNEL
0	0	1	0	SET LAST CHANNEL
0	0	1	1	RUN NOT LOADING FIFO
0	1	0	0	LOAD FIFO
0	1	0	1	RESET

BIT	DESCRIPTION	DAC DATA
15	CONTROL 3	
14	CONTROL 2	
13	CONTROL 1	
12	CONTROL 0	
11		SIGN
10		1K
9		512
8		256
7		128
6		64
5		32
4	ADDRESS 16	16
3	ADDRESS 8	8
2	ADDRESS 4	4
1	ADDRESS 2	2
0	ADDRESS 1	1

NOTE: System operates in the sequential mode. To operate on a single channel set First and Last Channel to the same address.

GENERAL OPERATION:

As shown in the TRUTH TABLE the four(4) MSB bits are system operating bits. The twelve(12) LSB bits are Data bits. An external system clock is required to operate this system.

EXAMPLE:
Load FIFO then run data out.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	RESET
0	0	0	1	SET DATA												SET FIRST CHANNEL
0	0	1	0	SET DATA												SET LAST CHANNEL
1	1	0	0	SET DATA												LOAD FIFO MEM LOC 0
1	1	0	0	SET DATA												LOAD FIFO MEM LOC n
0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	RUN

An external clock is required to start Data transfer. The next external clock will initiate load and transfer.
The DAC'S load at 600 nSec/ch. Transfer occurs when last channel is loaded. The system then waits for the next system clock, loads and transfers the next complete block of data. System WILL NOT transfer an uncompleted block of data.

EXAMPLE:
Run while loading data.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	RESET
0	0	0	1	SET DATA												SET FIRST CHANNEL
0	0	1	0	SET DATA												SET LAST CHANNEL
0	0	0	0	SET DATA												LOAD FIFO MEM LOC 0
0	0	0	0	SET DATA												LOAD FIFO MEM LOC 1
CONTINUE LOADING FIFO																

System will begin to transfer on first system clock after data is in the FIFO. It will load at data input speed until transfer is reached. After transfer is reached FIFO will load until next system clock occurs. If FIFO becomes FULL it will hold off the HANDSHAKE until a transfer start occurs and the FIFO writes Data out. If FIFO reaches an empty state, transfer WILL NOT occur until enough Data has been entered to complete a block (First channel to Last channel). Any System Clocks that occurs while FIFO is in an empty state WILL BE IGNORED.

```
[illegible]
```

DAC CALIBRATION

INTRODUCTION

The calibration of the LC DAC is easy.

1) Set code for 0---->0

2) Adjust zero pot for -10.000 Volts out.

3) Set code for +Full Scale (FS).

4) Set FS pot for +10.000 Volts out.

5) Calibration is complete.

DAC TEST REPORT

DAC MODEL LC DAC

Test Technician L.G.

Date 6-10-87

Register Number 50019

1.0 System Number 84900-00

2.0 Controller Number 84900-00

3.0 Serial Number RAD 034

4.0 Interface Type 12006

5.0 Logic Up-Date Rate 500 KHz

6.0 Data Code 2's COMP

7.0 Resolution 11 BITS AND SIGN

8.0 Accuracy ± ½ LSB

9.0 Output Full Scale ± 10V

10.0 Full Scale Settling Time 15 μS

11.0 Output Impedance < 1Ω UPTO 5mΩ

12.0 Options

GMDAC2 DATA SHEET CHANNEL # 0 S/N RAD 034

ANALOG OUTPUT = +/- 10.0000 VOLTS (FULL-SCALE)
RESOLUTION = 11 BITS PLUS SIGN.

BINARY DATA INPUT TWOS COMPLEMENT	THEORETICAL OUTPUT (VOLTS)	ACTUAL OUTPUT (VOLTS)	ERROR (MV)
0 1 1 1 1 1 1 1 1 1 1 1	+ 9.9951	9.9951	0
0 1 1 1 1 0 0 0 0 0 0 0	+ 9.3750	9.3754	+0.4
0 1 1 1 0 0 0 0 0 0 0 0	+ 8.7500	8.7505	+0.5
0 1 1 0 0 0 0 0 0 0 0 0	+ 7.5000	7.5005	+0.5
0 1 0 0 0 0 0 0 0 0 0 0	+ 5.0000	5.0003	+0.3
0 0 1 0 0 0 0 0 0 0 0 0	+ 2.5000	2.5002	+0.2
0 0 0 1 0 0 0 0 0 0 0 0	+ 1.2500	1.2500	0
0 0 0 0 0 0 0 0 0 0 1 0	+ 0.0098	0.0097	-0.1
0 0 0 0 0 0 0 0 0 0 0 0	+ 0.0000	+0.0000	0
1 1 1 1 1 1 1 1 1 1 1 1	- 0.0049	-0.0056	-0.7
1 1 1 1 1 0 0 0 0 0 0 0	- 0.6250	0.6252	-0.2
1 1 1 1 0 0 0 0 0 0 0 0	- 1.2500	1.2502	-0.2
1 1 1 0 0 0 0 0 0 0 0 0	- 2.5000	2.5002	-0.2
1 1 0 0 0 0 0 0 0 0 0 0	- 5.0000	5.0005	-0.5
1 0 1 0 0 0 0 0 0 0 0 0	- 7.5000	7.5007	-0.7
1 0 0 1 0 0 0 0 0 0 0 0	- 8.7500	8.7509	-0.9
1 0 0 0 1 0 0 0 0 0 0 0	- 9.3750	9.3759	-0.9
1 0 0 0 0 0 0 0 0 0 0 1	- 9.9951	9.9960	-0.9

DAC TEST REPORT

DAC MODEL LCDAC

Test Technician L.G.

Date 6-10-87

Register Number 50019

1.0 System Number 84900-00

2.0 Controller Number 84900-00

3.0 Serial Number RAD 035

4.0 Interface Type 12006

5.0 Logic Up-Date Rate 500KHz

6.0 Data Code 2's COMP

7.0 Resolution 11 BITS AND SIGN

8.0 Accuracy ± ½ LSB

9.0 Output Full Scale ± 10V

10.0 Full Scale Settling Time 15 μS

11.0 Output Impedance < 1Ω UPTO 5mΩ

12.0 Options

GMDAC2 DATA SHEET CHANNEL # 0 S/N RAD 035

ANALOG OUTPUT = +/- 10.0000 VOLTS (FULL-SCALE)
RESOLUTION = 11 BITS PLUS SIGN.

BINARY DATA INPUT TWOS COMPLEMENT		THEORETICAL OUTPUT (VOLTS)	ACTUAL OUTPUT (VOLTS)	ERROR (MV)
0 1 1 1 1 1 1 1 1 1 1 1	+	9.9951	9.9951	0
0 1 1 1 1 0 0 0 0 0 0 0	+	9.3750	9.3752	+0.2
0 1 1 1 0 0 0 0 0 0 0 0	+	8.7500	8.7501	+0.1
0 1 1 0 0 0 0 0 0 0 0 0	+	7.5000	7.5001	+0.1
0 1 0 0 0 0 0 0 0 0 0 0	+	5.0000	5.0001	+0.1
0 0 1 0 0 0 0 0 0 0 0 0	+	2.5000	2.5000	0
0 0 0 1 0 0 0 0 0 0 0 0	+	1.2500	1.2500	0
0 0 0 0 0 0 0 0 0 0 1 0	+	0.0098	0.0097	-0.1
0 0 0 0 0 0 0 0 0 0 0 0	+	0.0000	+0.0000	0
1 1 1 1 1 1 1 1 1 1 1 1	-	0.0049	-0.0047	0.2
1 1 1 1 1 0 0 0 0 0 0 0	-	0.6250	0.6247	+0.3
1 1 1 1 0 0 0 0 0 0 0 0	-	1.2500	1.2498	+0.2
1 1 1 0 0 0 0 0 0 0 0 0	-	2.5000	2.4998	+0.2
1 1 0 0 0 0 0 0 0 0 0 0	-	5.0000	4.9999	+0.1
1 0 1 0 0 0 0 0 0 0 0 0	-	7.5000	7.4999	+0.1
1 0 0 1 0 0 0 0 0 0 0 0	-	8.7500	8.7500	0
1 0 0 0 1 0 0 0 0 0 0 0	-	9.3750	9.3749	+0.1
1 0 0 0 0 0 0 0 0 0 0 1	-	9.9951	9.9951	0

DAC TEST REPORT

DAC MODEL LCDAC

Test Technician L.G.

Date 6-10-87

Register Number 50019

1.0 System Number 84900-00

2.0 Controller Number 84900-00

3.0 Serial Number RAD 036

4.0 Interface Type 12006

5.0 Logic Up-Date Rate 500 KHz

6.0 Data Code 2's COMP

7.0 Resolution 11 BITS AND SIGN

8.0 Accuracy ± ½ LSB

9.0 Output Full Scale ± 10V

10.0 Full Scale Settling Time 15 μS

11.0 Output Impedance < 1Ω UPTO 5mΩ

12.0 Options

GMDAC2 DATA SHEET CHANNEL # 0 S/N RAD 036

ANALOG OUTPUT = +/- 10.0000 VOLTS (FULL-SCALE)
RESOLUTION = 11 BITS PLUS SIGN.

BINARY DATA INPUT TWOS COMPLEMENT	THEORETICAL OUTPUT (VOLTS)	ACTUAL OUTPUT (VOLTS)	ERROR (MV)
0 1 1 1 1 1 1 1 1 1 1 1	+ 9.9951	99950	-0.1
0 1 1 1 1 0 0 0 0 0 0 0	+ 9.3750	9.3754	+0.4
0 1 1 1 0 0 0 0 0 0 0 0	+ 8.7500	8.7507	+0.7
0 1 1 0 0 0 0 0 0 0 0 0	+ 7.5000	7.5006	+0.6
0 1 0 0 0 0 0 0 0 0 0 0	+ 5.0000	5.0005	+0.5
0 0 1 0 0 0 0 0 0 0 0 0	+ 2.5000	25003	+0.3
0 0 0 1 0 0 0 0 0 0 0 0	+ 1.2500	12502	+0.2
0 0 0 0 0 0 0 0 0 0 1 0	+ 0.0098	00099	+0.1
0 0 0 0 0 0 0 0 0 0 0 0	+ 0.0000	+0.0001	+0.1
1 1 1 1 1 1 1 1 1 1 1 1	- 0.0049	-00053	-0.4
1 1 1 1 1 0 0 0 0 0 0 0	- 0.6250	-06249	+0.1
1 1 1 1 0 0 0 0 0 0 0 0	- 1.2500	-12497	+0.3
1 1 1 0 0 0 0 0 0 0 0 0	- 2.5000	-24997	+0.3
1 1 0 0 0 0 0 0 0 0 0 0	- 5.0000	-49994	+0.1
1 0 1 0 0 0 0 0 0 0 0 0	- 7.5000	-75001	-0.1
1 0 0 1 0 0 0 0 0 0 0 0	- 8.7500	-87501	-0.1
1 0 0 0 1 0 0 0 0 0 0 0	- 9.3750	-93755	-0.5
1 0 0 0 0 0 0 0 0 0 0 1	- 9.9951	-99952	-0.1

DAC TEST REPORT

DAC MODEL LCDAC

Test Technician L.G.

Date 6-10-87

Register Number 50019

1.0 System Number 84900-00

2.0 Controller Number 84900-00

3.0 Serial Number RAD037

4.0 Interface Type 12006

5.0 Logic Up-Date Rate 500KHz

6.0 Data Code 2's COMP

7.0 Resolution 11 BITS AND SIGN

8.0 Accuracy ± ½ LSB

9.0 Output Full Scale ± 10V

10.0 Full Scale Settling Time 15μS

11.0 Output Impedance < 1Ω UPTO 5ma

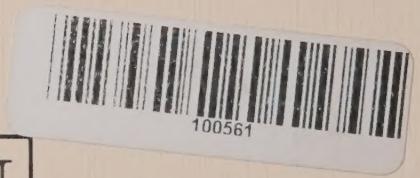
12.0 Options

GMDAC2 DATA SHEET CHANNEL # 0 S/N RAD037

ANALOG OUTPUT = +/- 10.0000 VOLTS (FULL-SCALE)
RESOLUTION = 11 BITS PLUS SIGN.

BINARY DATA INPUT TWOS COMPLEMENT	THEORETICAL OUTPUT (VOLTS)	ACTUAL OUTPUT (VOLTS)	ERROR (MV)
0 1 1 1 1 1 1 1 1 1 1 1	+ 9.9951	9.9952	+0.1
0 1 1 1 1 0 0 0 0 0 0 0	+ 9.3750	9.3752	+0.2
0 1 1 1 0 0 0 0 0 0 0 0	+ 8.7500	8.7504	+0.4
0 1 1 0 0 0 0 0 0 0 0 0	+ 7.5000	7.5004	+0.4
0 1 0 0 0 0 0 0 0 0 0 0	+ 5.0000	5.0003	+0.3
0 0 1 0 0 0 0 0 0 0 0 0	+ 2.5000	2.5001	+0.1
0 0 0 1 0 0 0 0 0 0 0 0	+ 1.2500	1.2499	-0.1
0 0 0 0 0 0 0 0 0 0 1 0	+ 0.0098	0.0098	0
0 0 0 0 0 0 0 0 0 0 0 0	+ 0.0000	0.0000	0
1 1 1 1 1 1 1 1 1 1 1 1	- 0.0049	-0.0056	-0.7
1 1 1 1 1 0 0 0 0 0 0 0	- 0.6250	0.6256	-0.6
1 1 1 1 0 0 0 0 0 0 0 0	- 1.2500	1.2504	-0.4
1 1 1 0 0 0 0 0 0 0 0 0	- 2.5000	2.5003	-0.3
1 1 0 0 0 0 0 0 0 0 0 0	- 5.0000	5.0005	-0.5
1 0 1 0 0 0 0 0 0 0 0 0	- 7.5000	7.5007	-0.7
1 0 0 1 0 0 0 0 0 0 0 0	- 8.7500	8.7509	-0.9
1 0 0 0 1 0 0 0 0 0 0 0	- 9.3750	9.3760	-1.0
1 0 0 0 0 0 0 0 0 0 0 1	- 9.9951	9.9959	-0.8

Preston Scientific
Leaders in the development and manufacture of precision amplifiers and analog-to-digital conversion systems since 1959.



PRESTON

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